PRESCOUTER

Research Support Service

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What are some of the applications for chemical-mechanical planarization (CMP)?

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Intelligence Brief Question

What are some of the applications for chemical-mechanical planarization (CMP) and who are some of the leading organizations and research groups working on this topic today?

Executive Summary

The PreScouter team was tasked with understanding and presenting the key applications for CMP and to highlight potential research partners to a client in the manufacturing sector. To do this, PreScouter:

- **Identified several applications for this technique**, providing for each identified application:
    - Description of how CMP is utilized
    - Benefits of this technique
    - Differentiators for specific applications
    - High level trends of CMP for this application
- **Identified centers of excellence globally in CMP research**, providing for each identified center/research group:
    - List of relevant research articles and patents pertaining to CMP
    - Description of research efforts/goals
    - Highlight industry partners
    - Highlight roadblocks to evolution of CMP technology

Executive Summary

Overview:

Chemical mechanical planarization (CMP) was originally developed to overcome processing issues in microelectronics manufacturing, such as planarization of interlayer dielectric materials. The technology was then extended to **enable the manufacturing of structures that were impossible or difficult to build**, for example, for multilevel constructions like micromotors, gears, or micromirrors.

Main Applications:

The applications of CMP are varied and spread out in the electronics industry.

- The major application is understandably in the **integrated circuit manufacturing** industry.
- It is also playing an increasingly important role in different applications such as **micro-electro-mechanical systems (MEMS) and optics**.

Executive Summary

Key Insights:

There are two major applications of CMP in ultra-large-scale integrated manufacturing:

- To smooth surface topography of inter-level dielectrics (ILD, usually silicon dioxide)
- To remove excess material to produce inlaid metal structure or isolation trenches.

The CMP process is a known method to finely polish wafers for chip production. In this process, polishing agent suspensions are used to machine the material. These suspensions have a chemical effect on the layer being polished as well as a mechanical, abrasive effect on the surface of the wafer.

- The grain size distribution of these suspensions must be precisely defined in order to obtain the appropriate fluidity in the process.
- Of primary importance is to eliminate oversized particles of any kind in order to prevent flaws caused by scratches.

Overview of the

CMP Technology & Market

CMP Technology

Overview

CMP has grown from its invention in 1984, to one of the fastest growing segments of the semiconductor equipment industry. In 1997 the growth rate of CMP equipment averaged 30% in comparison with the rest of the semiconductor equipment market. The factors that enabled this dynamic growth include both the technical advantages of CMP and the history of its development and subsequent spread into the industry. The growth of CMP technology has spawned new business and supplier networks as well as new fields of study that pose new challenges to be solved.

Drawbacks

Improvements in wafer metrology are sought after to tackle problems that continuously arise such as stress cracking, delaminating at weak interfaces and corrosive attacks from slurry chemicals.

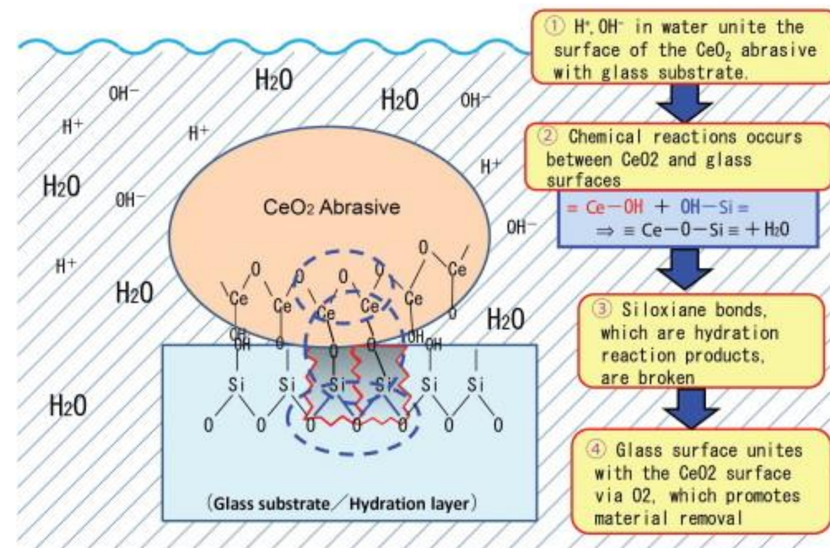

Figure: Potential problems can occur during slurry chemical use. Source: Science Direct

CMP Technology

Drawbacks

In addition, the popular oxide polishing process faces a stern challenge in its lack of end points needing blind polishing. This makes it hard to determine when the necessary amount of planarization has been achieved.

This is **time-consuming** and **increases costs**.

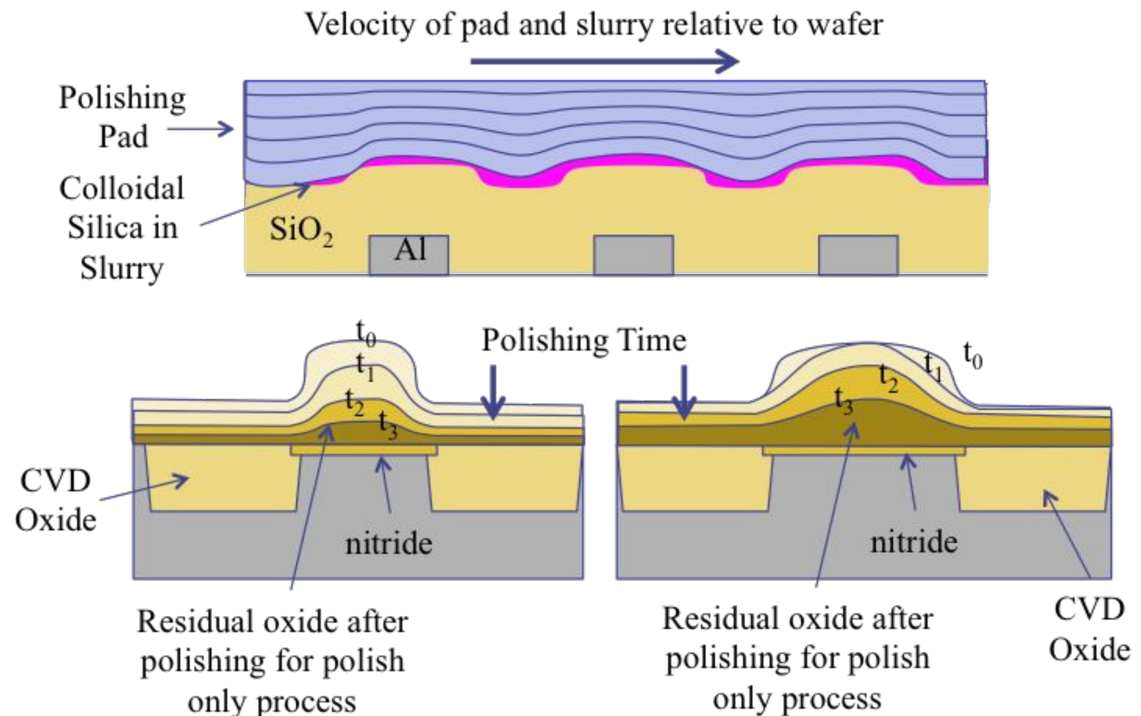

Figure. The oxide polishing process. Source: Semi-Tracks.

CMP Technology

The Future

One of the major factors that is currently driving the CMP market is the growing use of the CMP process in the **semiconductor industry**. It is one of the processes while manufacturing ICs and chips, compound semiconductor among many others.

Governments around the world are increasingly supporting **digitalization**, eventually promoting the usage of various electronic devices among consumers such as smartphones, tablets and other electronic devices.

This is anticipated to support the semiconductor industry along with with its parent market i.e., the consumer electronics market globally.

The growing use of MEMS technology in the various **microscopic devices** is also expected to fuel the growth of the CMP market.

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2. https://www.sciencedirect.com/topics/materials-science/chemical-mechanical-planarization
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Overview of

Relevant Applications for CMP

Planar Thin Films for Non-IC Applications

Overview

Nearly every laptop or desktop computer in use today contains one or more hard disk drives. Every mainframe server and supercomputer is normally connected to hundreds of them. Now even DVR, iPod, and camcorders use hard disks instead of tape or flash memory. The computer hard drives store changing digital information on rigid magnetic memory disks.

In order to deposit the magnetic materials properly, the substrate must be perfectly flat and free of defects such as pits, scratch, and bumps. Any of these defects not only lower the effectiveness of the magnetic layer to store the information but also can cause the crash of read– write heads that are flying over the platen at a tremendous speed and impressive low altitude.

The operation can be compared to a situation where a large aircraft is flying at the top speed, less than a meter above the ground. Any nano asperity on the computer hard drive disk is equivalent to an insurmountable mountain for the aircraft to avoid. Therefore, a CMP process has been used to planarize the substrates for the computer hard drives.

Figure. A hard disk drive platter. Source: Wikipedia.

Planar Thin Films for Non-IC Applications

Fabrication Process

There are two major types of substrates used in today's computer hard drives. One is glass based: ceria (CeO_2) particles are the most commonly used abrasive for this application. The other is aluminum coated with NiP. The NiP layer is usually electrochemically plated and then subsequently planarized with alumina-based slurry followed by silica-based slurry to remove the defects and nano asperities.

The surface roughness after the CMP process is often required to be less than 1 A˚.

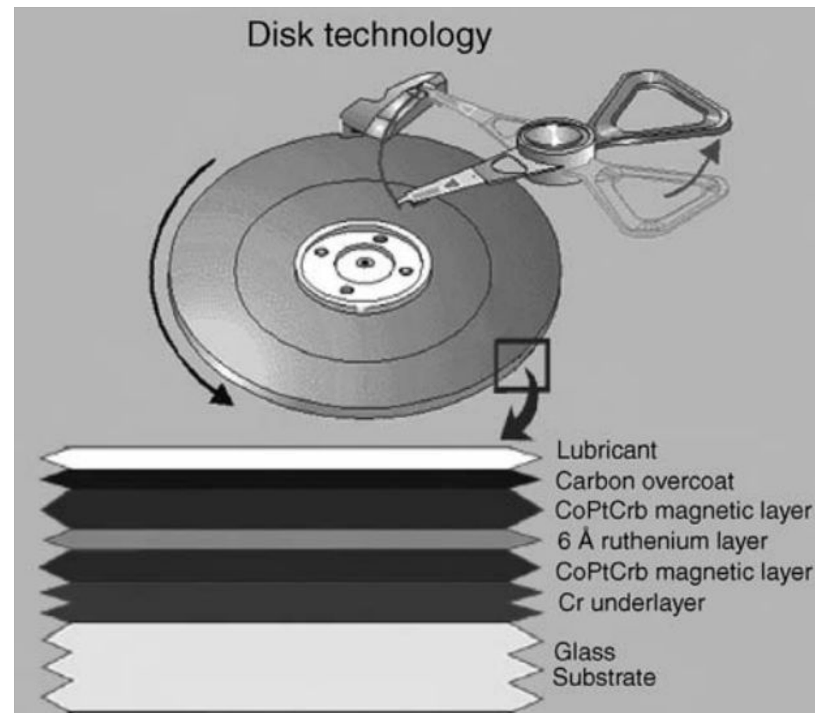
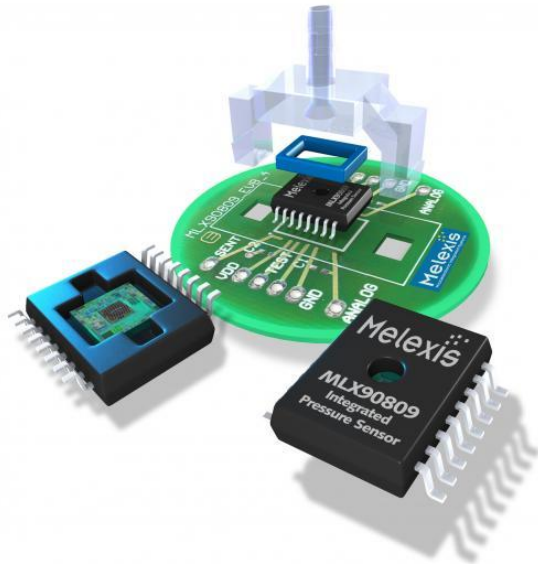


Figure. A cross section of a typical computer hard drive disk.

Integrated Pressure Sensor

Overview

The term **integrated sensor** describes the technology when MEMS structures and signal processing circuits are combined on the same chip. For the fabrication of an integrated pressure sensor, a CMOS circuit for signal processing had first been produced on the wafer front side. As shown schematically in the figure (next page), a silicon nitride membrane structure on the front side has to be opened subsequently by a selective silicon wet etching process from the wafer backside using KOH. The size of the membrane is defined by the size of the opening in the SiNx etch mask and the thickness of the substrate.



The lithography for the definition of the SiNx etch mask opening and the subsequent RIE step requires a polished wafer backside. This can be accomplished by the use of **double-side polished wafers** that, however, show some disadvantages like handling and chucking problems with standard semiconductor manufacturing equipment. Therefore, the CMOS circuit has been processed using standard 150-mm wafers with unpolished backside. Afterwards, the substrates were thinned to the required thickness by grinding and subsequently smoothed by CMP.

Integrated Pressure Sensor

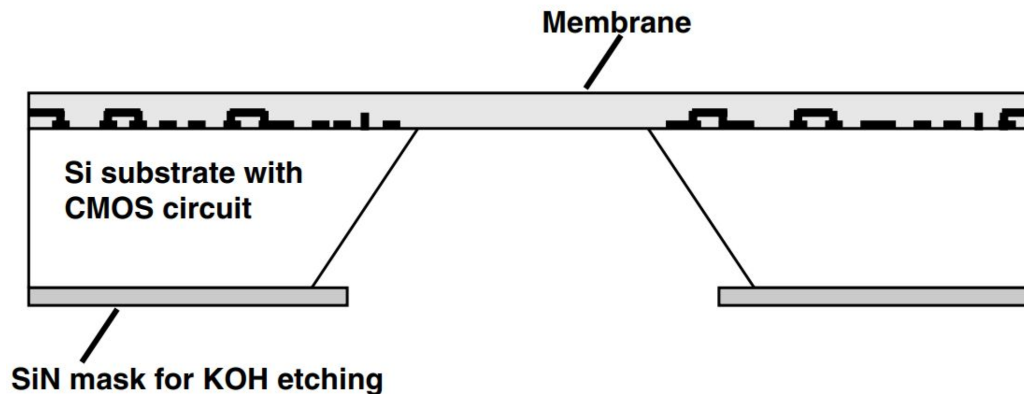


Figure. Schematic of integrated pressure sensor in bulk micromachining.

Fabrication Process

- After front-side protection of the finished CMOS circuits by means of grinding tape or photoresist, the wafers were ground from 675 to 503mm thickness using a two-step grinding process with #300 and #2000 grinding wheels. As the wafer thickness defines the size of the membranes, the uniformity of the grinding process must not exceed a total thickness variation (TTV) of 3.0 mm in the case of this example.
- A subsequent two-step Si CMP process using colloidal silica with an additive in order to enhance polishing rate, which had originally been developed for Si wafer manufacturing, removed 3.0–3.5mm of silicon from the wafer backside.

Integrated Pressure Sensor

Fabrication Process (cont'd)

- The removal of about 3mm by CMP led to a sufficient clearing of the subsurface damage of the grinding process, indicated by minimal undercut variation of the following KOH anisotropic etch. The necessary damage layer removal of about 3mm by polishing corresponds well with the results from other groups developing technologies for wafer thinning, chip stacking, and packaging.
- Polishing and cleaning quality has been controlled with a laser surface particle counter (eg. Surfscan) by using the haze measurement option, which is a measure of surface microroughness. After removal of the front-side protection, deposition and structuring of the SiNx mask, and exposure of the pressure sensor membranes by KOH etching, the wafers have to be sealed hermetically with cap wafers using wafer bonding. Finally, the chips are separated by wafer sawing.

Additional Information

In addition to integrated pressure sensors, the described technology for the formation of membranes by bulk micromachining can also be used for the fabrication of integrated airflow sensors, MEMS microphones, and other related devices.

Poly-Si Surface Micromachining and Angular Rate Sensor

Overview

One of the earliest applications of CMP for microfabrication was the pioneering work at Sandia with the planarization of polysilicon for poly-Si surface micromachining. The motivation for CMP was the elimination of topography caused by the stacking of several structured layers. The **Sandia Ultraplanar, Multilevel MEMS Technology (SUMMiT^{TM})** fabrication process with up to four CMP-planarized mechanical layers has been successfully used to build MEMS gear systems, planar pressure sensors, and other devices employing high-aspect-ratio micromachining.

By using the example of an angular rate sensor (gyro), developed and fabricated at the author's lab, the requirements of a CMP process for polysilicon micromachining will be discussed in detail in the following. Gyros are employed in growing quantities for automotive applications like GPS navigation systems or anti-skid and rollover protection systems, and also in cameras for image stabilization or in hard-disk drives for read/write head protection.

Poly-Si Surface Micromachining and Angular Rate Sensor

Relevant Images

Figures 1 and 2 show closeups of poly-Si micromachines from **Sandia Labs**, manufactured by using several poly-Si CMP processes. Figure 1 depicts the gear wheels of a 10:1 transmission. Due to CMP, the gears are completely planar. Figure 2 shows the alignment clips for positioning the gears. The two layers of gears are clearly visible.

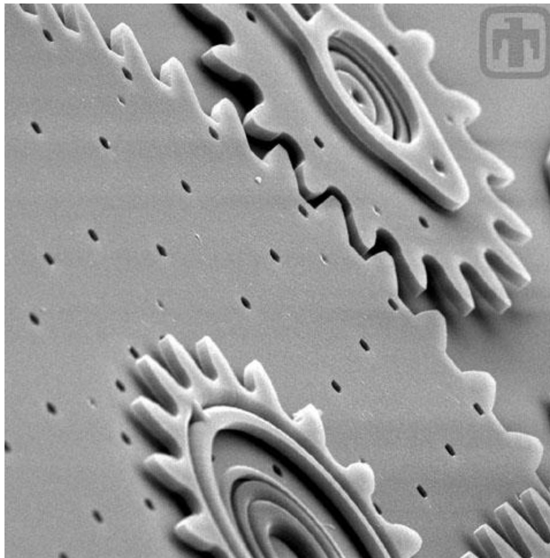


Figure 1. Gear wheels

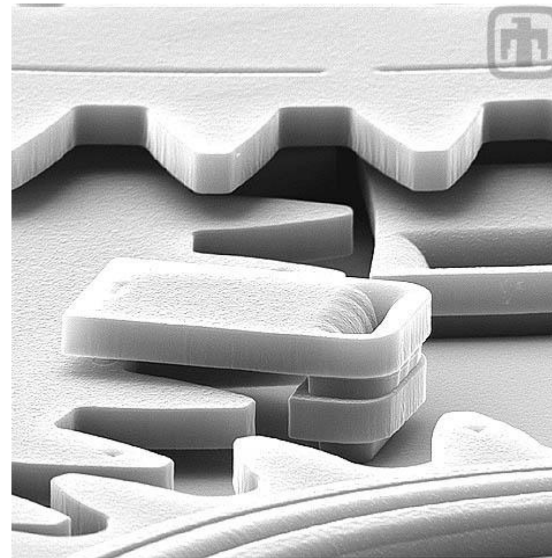


Figure 2. Alignment clips

Poly-Si Surface Micromachining and Angular Rate Sensor

Fabrication Process

A gyro sensor consists of a ring/disk structure that is performing circular vibrations around an axis perpendicular to the picture plane. The vibrating ring/disk structure as well as the drive mechanism consists of 11-mm-thick poly-Si, which has been structured by deep RIE and released from the sacrificial oxide layer underneath by HF vapor phase etching.

For the deposition of the thick poly-Si, a modified epitaxy deposition process (EPI poly) has been used. However, as can be seen in Fig. 4, the deposition process leads to a rough poly-Si surface with Ra 100nm. For the removal of underlying topography, the surface has to be planarized by CMP in order to enable high-resolution lithography and etching.

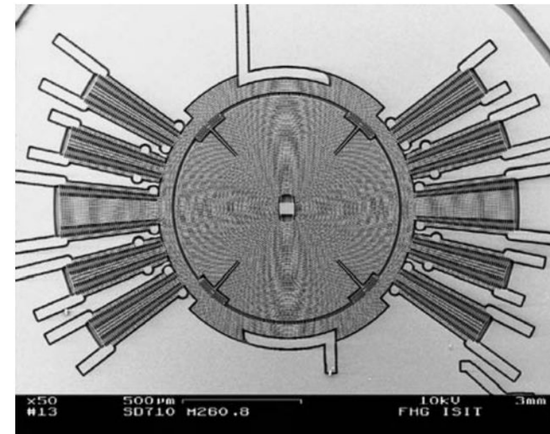


Fig.3. Structure of the angular rate sensor (gyro)

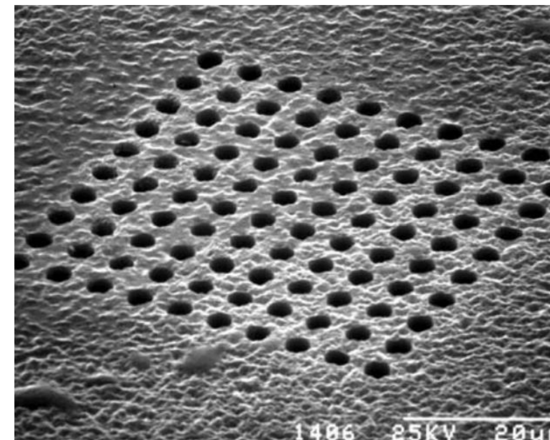
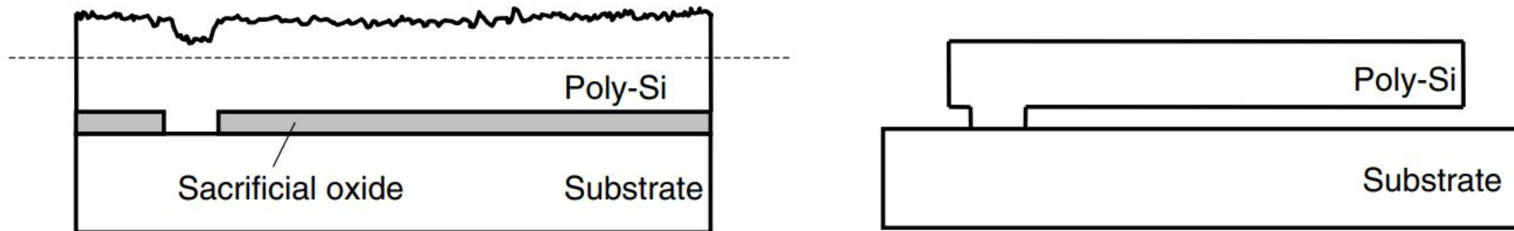


Fig. 4. Roughness of a 10-µm-thick EPI-poly layer.

Poly-Si Surface Micromachining and Angular Rate Sensor

Fabrication Process



The above figure shows schematically the roughness removal by means of CMP and the released structures after HF vapor-phase sacrificial oxide etching. The polysilicon thickness after CMP and its homogeneity over the wafer is very critical, as it has direct influence on sensitivity, measurement range, and total yield.

Poly-Si Surface Micromachining and Angular Rate Sensor

Additional Information

- The poly-Si thickness of the EPI-poly deposition process is a compromise between underlying topography, processing time, and nonuniformity of the deposition and polishing processes.
- A reasonable start thickness is 14mm; that is, 3mm has to be removed by CMP. For the poly-Si CMP process, a fumed silica based alkaline slurry has been used which achieved a removal rate of about 500nm/min and leads to a final roughness of $R_a \cong 0.3-0.5$nm.
- The thickness is measured by using an adapted reflectometer that, however, requires a smooth surface. Therefore, the control wafers had to be pre-polished before they could be used for removal rate determination.

Infrared Digital Micromirror Array

Overview

Microfabricated devices capable of switching optical light beams, also termed MOEMS, have gained attention about two decades ago for applications like optical fiber switches, microscanners, or digital micromirror arrays. Particularly, the latter devices have found widespread application in video projection systems for office presentations, home cinema, and very recently, the replacement of classical projectors in movie theaters. Other applications, for example, for head-up displays on auto windscreens are in development. In all cases, arrays of small micromirrors are used for the modulation of light.

As the optical mirrors require planar surfaces, CMP is regularly employed in the manufacturing sequence. Two examples of light modulators, based on arrays of tilting micromirrors are explained in the following. The first example is a **commercially available digital micromirror device (DMD) from Texas Instruments (TI)** for video projectors, using one CMP step for micromirror fabrication. The second example is a **micromirror array for switching IR light**, which needs three CMP steps in the manufacturing process flow.

Infrared Digital Micromirror Array

Fabrication Process

The figure shows a cut through the TI device displaying the design of the MEMS-based DMD. The mirrors can be tilted by electrostatic forces by means of address and bias voltage applied to the mirrors and yokes. The structures are manufactured by a sequence of appropriate deposition and structuring processes.

TI uses hardened photoresist as a sacrificial material, which is later removed by a dry etch step to form the air gaps to release up to 1.3 million 16mm16mm mirrors. The only CMP step is the planarization of a thick oxide film, deposited over the metal-2 level of the underlying CMOS device, which mainly consists of SRAM address circuits.

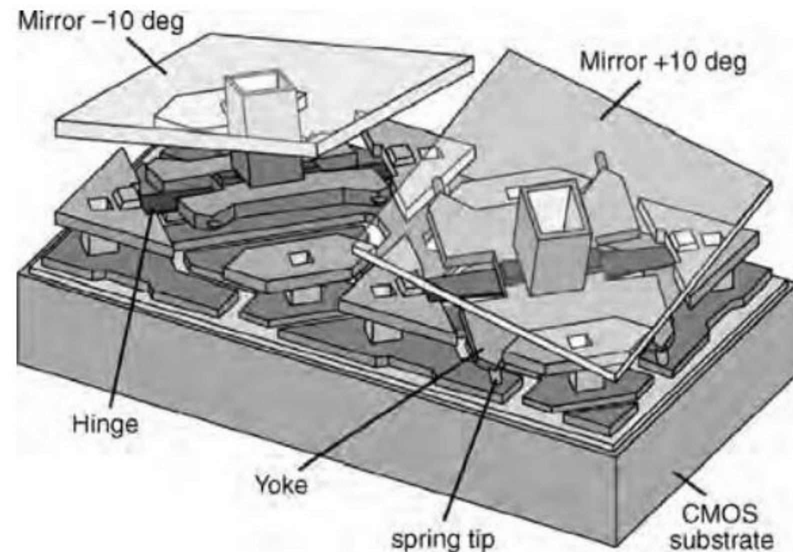


Figure. Illustration of two tilted micromirrors of TI's digital micromirror device.

Infrared Digital Micromirror Array

Fabrication Process

- In the following, a metal surface micromachining technology for the manufacturing of a 256 x 256 digital micromirror array of an integrated infrared imaging system using Ni as a structural material and Cu as a sacrificial layer will be presented. The process flow consists of three planarization steps and gives a nice synopsis of CMP applications in microfabrication.
- The 64k, 80µm x 80µm sized tilting mirrors are built on the top of a CMOS based control ASIC. In order to reduce the topography of the underlying metallization/passivation structures, a 2.5 µm-thick PECVD oxide film is first deposited on the ASIC.
- An ILD oxide CMP step based on Klebosol™ 30N50 colloidal silica slurry is used for planarization. In order to connect the ASIC with the deflection electrodes above (pg 25), vias have to be etched into the planarized dielectric film. Then, a copper metal stack including a TaN barrier has to be deposited and a two-step Cu damascene CMP process has to be performed. As this process is equivalent to Cu damascene in microelectronics fabrication, standard Cu CMP slurries can be used.
- The wedge-shaped deflection electrodes and the 7µm high posts for the suspension of the mirrors consist of Ni, fabricated by using 3D electroplating. The complete wafer surface is then covered with a Cu seed layer that has been reinforced by Cu electroplating to 10µm thickness.

Infrared Digital Micromirror Array

Fabrication Process

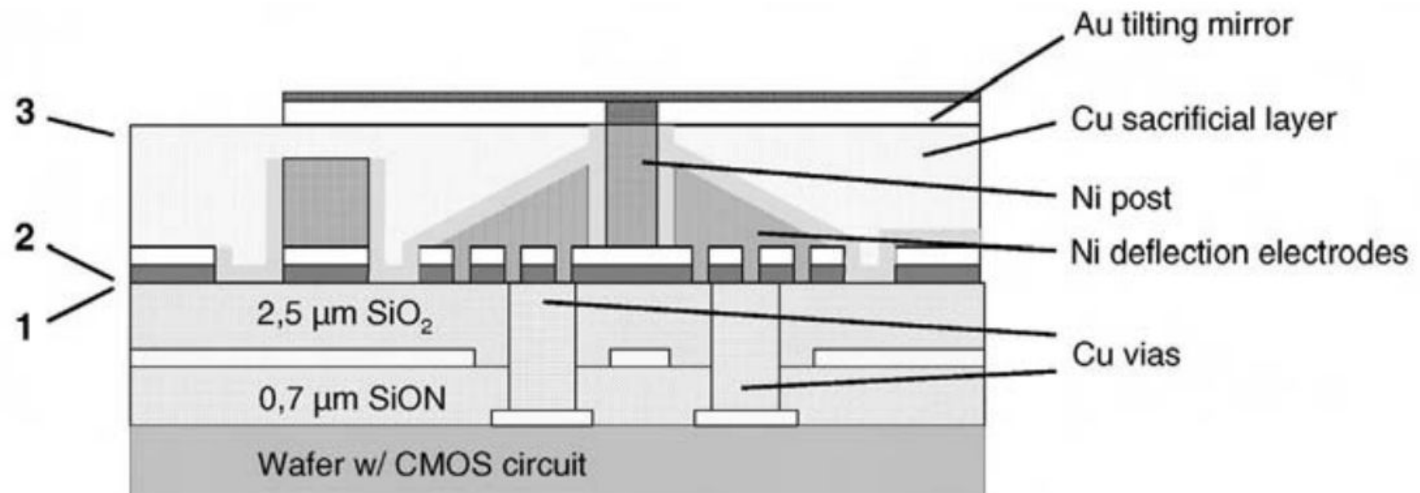


Figure. Schematic cut-through of the micromirror device. Three CMP steps have to be performed: (1) oxide planarization of CMOS passivation, (2) Cu damascene of vias, and (3) CMP of thick Cu sacrificial layer until the Ni posts are exposed.

- The third CMP step removes and planarizes the Cu layer until the Ni posts are exposed. This Cu CMP process has to fulfill the requirements of high selectivity to nickel in order to avoid Ni recess and very low copper dishing between the nickel posts in order to achieve flat mirrors.

Infrared Digital Micromirror Array

Additional Information

On top of the exposed nickel posts, a gold film has been deposited and structured to form the micromirrors. Subsequently, a wet etch process selective to gold and nickel clears the underlying copper sacrificial layer. This step releases the mirrors and allows them to tilt by means of electrostatic forces by applying a control voltage at the deflection electrodes. The figure below shows some mirrors of the array and a closeup view of the cell structure, which depict mirrors, wedged electrodes and posts for suspension of the torsion hinges.

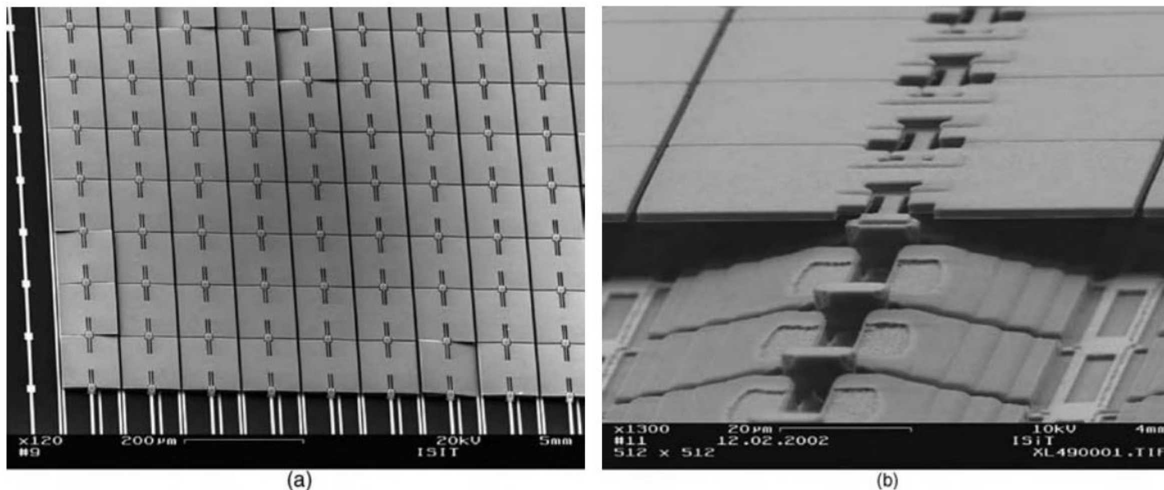


Figure: (a) Micromirror array, fabricated in metal surface micromachining. (b) Closeup view of micromirror device. Gold mirror plates and nickel wedged deflection electrodes are clearly visible.

MEMS Mirror-based Laser Scanning Projector

Overview

Biaxial MEMS mirror laser scanners are very interesting for the realization of compact projection systems, for example, for head-up displays in cars or for pico projectors in mobile phones. These can be very compact as only one mirror is needed to scan the three beams of an RGB laser in the x and y directions. Using laser beams has the advantage that no projection lens is needed and the picture is always in focus. Similar to cathode ray tubes, the beam is scanned fast in the horizontal direction to write the lines and more slowly in the vertical direction to generate the pictures.

MEMS Mirror-based Laser Scanning Projector

Overview

The figure below shows a schematic of the electrostatically driven mirror with two directions of deflection. The fast moving mirror is fixed by torsion springs at a gimbal and is excited to oscillate by an electrostatic drive, realized by stacked comb electrodes. The gimbal itself is also fixed by torsion springs to the MEMS chip and is excited to oscillate more slowly to perform the vertical sweep. The mirror has a diameter of 0.9 mm and oscillates in resonance with 32 kHz as fast axis frequency and with 0.6 kHz as slow axis frequency.

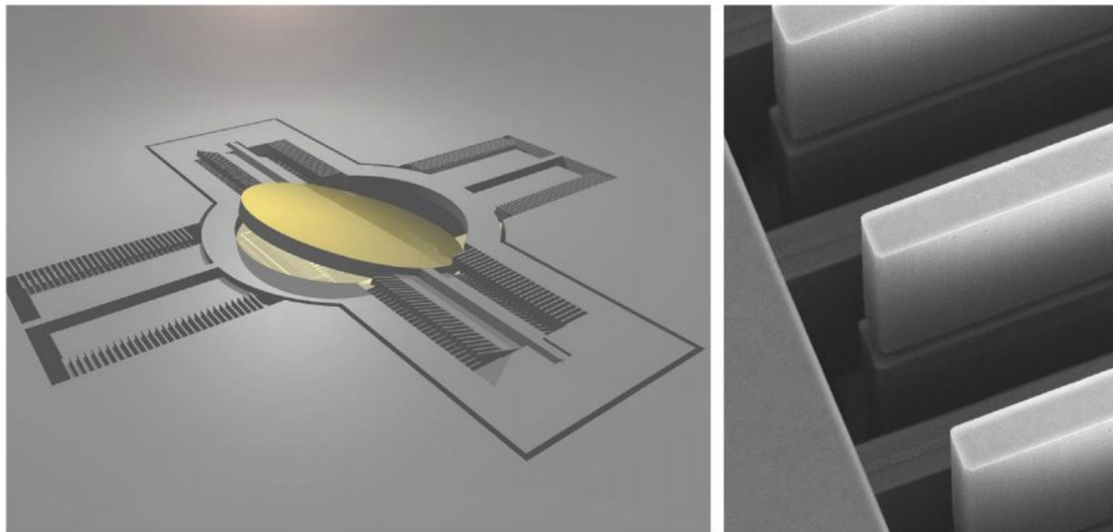


Figure: Schematic illustration of the two-axis scanning mirror of the laser scanning projector and details of the comb electrodes.

MEMS Mirror-based Laser Scanning Projector

Fabrication Process

- A schematic of the fabrication process is shown in the below figure. After oxidation of the double-side polished silicon substrate wafer, a first lower poly-Si layer with a thickness of 45 mm is deposited by means of an epi-poly process.
- In order to remove spikes and obtain a smooth surface, 5 mm of poly-Si has to be removed by poly-Si CMP. This polishing is a two-step process, consisting of a 5 mm bulk removal by means of a fumed silica slurry and a subsequent final polish of several 10 nm with a haze-free slurry.
- After deposition and structuring of some intermediate layers, a second upper polySi layer, again with a thickness of 45 mm, is deposited and subsequently polished with the same two-step poly-Si CMP process. As this will be the surface of the evaporated silver mirror, a smooth as well as flat surface has to be achieved.

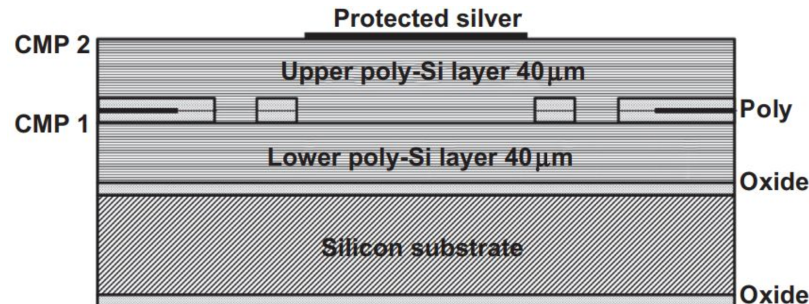


Figure: Fabrication steps: two 40 mm thick poly-Si layers are needed for the mirror and the electrostatic deflection comb structures.

MEMS Mirror-based Laser Scanning Projector

Fabrication Process

- After a backside silicon etch and the removal of the sacrificial layer, the scanning mirror device is released, as seen in the present figure.

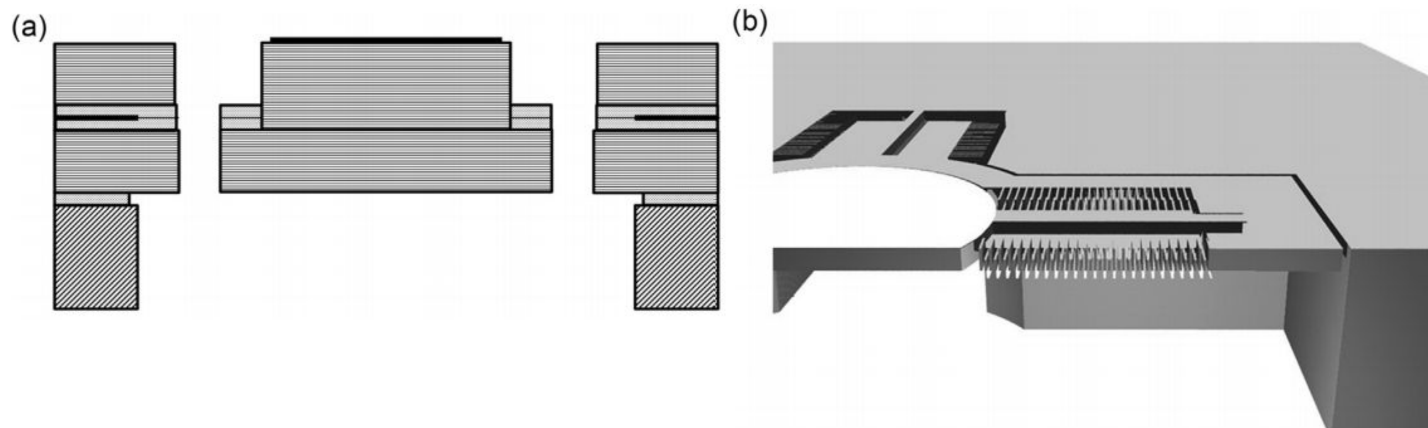


Figure: Schematic cross-section through scanning mirror MOEMS (a) and 3D illustration of the device (b).

- As the scanning mirror device is operating in resonance for both deflection directions, it has to be packaged under vacuum using high-vacuum WLP. Two caps are needed, a backside wafer to seal the lower chamber and a transparent front cap.

MEMS Mirror-based Laser Scanning Projector

Additional Information

The backside wafer, which also includes an integrated Ti-getter layer to maintain the high vacuum, is bonded against the smooth surface of the device wafer by using Au/Si eutectic bonding and the glass cap wafer is bonded using glass frit bonding. In order to avoid parasitic reflections, the glass lid is not parallel with the device surface but slightly tilted.

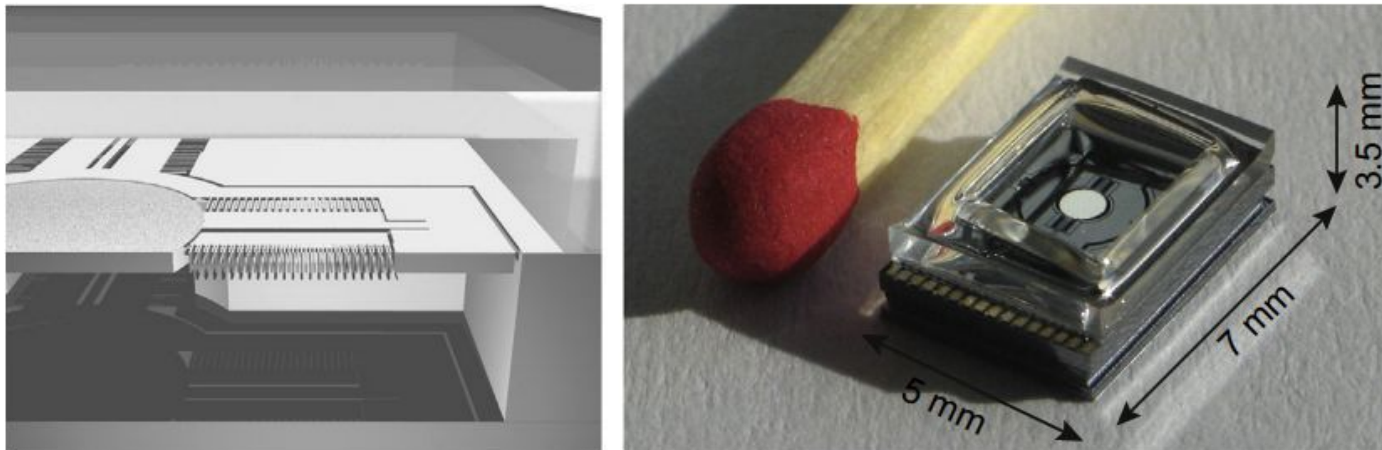


Figure: Schematic of the packaged MEMS scanning mirror device using front and backside high-vacuum WLP and Photograph of the finished device.

Comparison of CMP Requirements for Microelectronics Manufacturing with Microfabrication

Parameters	Microelectronics	Microfabrication	Comparison	Comments
Layers	Various SiO_2, poly-Si, W, Cu, noble metals	Various SiO_2, poly-Si, Si, various metals, ceramics, polymers	Great variety	Upcoming materials: PZT, magnetic alloys
Typical layer thickness	~0.1–2.0 µm	~0.2–50 µm	Larger	
Required CMP removal	~0.1–1.5 µm	~0.1–20 µm	Larger	
Required polishing rate	0.2–0.5 µm/min	>0.5 µm/min	Higher	New consumable sets, rougher processes required. Alternative: grind/polish sequence
Nonuniformity	<2 %	1–5 %	Relaxed	Exception: functional layer defines device properties. dependency on deposition NU
Edge exclusion	Down to 1.5 mm	Typ. 6 mm	Relaxed	Due to use of older equipment generations
CMP tool throughput	20–50 wafers/h	<10 wafers/h	Relaxed	
Pattern width	Down to 65 nm	µm–mm	Larger	
Lithography	Optical, 193 nm, DOF 0.5 µm	Optical, g- or i-line, DOF 5 µm e-beam, X-ray, DOF 5–50 µm	Specific	
Required planarity	<100 nm	>100 nm	Relaxed	Exception: optoMEMS: $<\lambda/10$
Topography	Maximum 1 µm	1–10 µm	Larger	
Dishing	<50 nm	>100 nm	Relaxed	Problem: mm-scale patterns
Erosion	<50 nm	>100 nm	Relaxed	Depending on pattern density
Roughness	Some nm	10 nm	Relaxed	Exception: wafer bonding ≈0.5 nm
Particle size	>32 nm	Pattern-size dependent	Relatively uncritical	

Comparison of CMP Requirements for Microelectronics Manufacturing with Microfabrication

Parameters	Microelectronics	Microfabrication	Comparison	Comments
Particle density	$<0.02/cm^2$	Die-size dependent	Relatively uncritical	Exception: wafer bonding $<1/cm^2$
Surface contamination	$<1 \times 10^{10}/cm^2$	CMOS: $<5 \times 10/cm^2$ Mechanical devices: product specific	Uncritical	Wafer bonding and BioMEMS need "clean surface"
Substrates	Si, SOI, III–V semiconductors	Si, metal, glass, quartz, ceramics	Greater variety	
Substrate size	200–300 mm	100—max 200 mm	Smaller	Production: lower unit numbers
Substrate thickness	Production: 500–800 µm Finishing: down to 50 µm	production: 200–700 µm Finishing: down to 20 µm	Specific	

CMP Market

- The global CMP slurry market was valued at 790 million USD in 2018 is expected to reach 1080 million USD by the end of 2025, growing at a **CAGR of 4.0%** during 2019-2025.
- The major factors driving the growth of the CMP market during the forecast period are the growing need of CMP for wafer planarization, high demand for consumer electronic products, and increasing use of micro-electro-mechanical systems (MEMS). CMP has been used for the mass production of microsystems for a number of decades now.

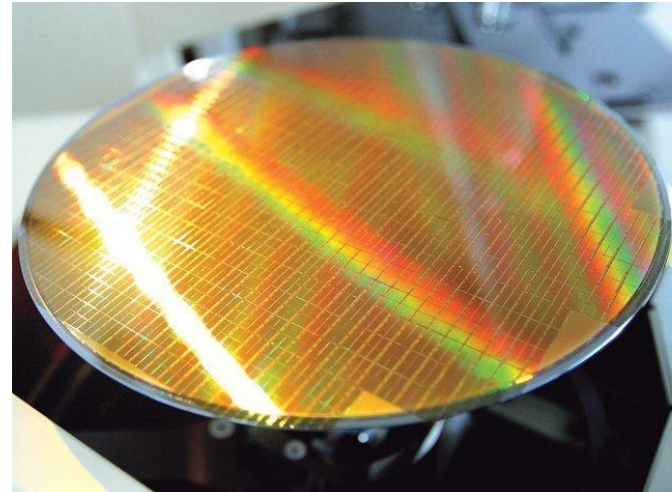


Figure: A CMP polished wafer

Overview of

Global Centers of Excellence in CMP

Hwatsing

HWATSING 华海清科

Overview

Chemical Mechanical Planarization (CMP) is widely used in polishing an array of products, including cell phone screens and the mirror-like aluminum alloy back plates. However, Tianjin Hwatsing Technology Company Limited (Hwatsing) is the only company in China capable of developing 12 inch (300mm) copper polishing equipment. It is the owner of several patented technologies, and enjoys a formidable reputation in CMP research and development, as well as the industrialization of equipment manufacturing.

The company was established in 2013 and is a high-tech enterprise jointly invested by the Tianjin Government and Tsinghua University (although Tsinghua University separately conducts its own CMP research alongside its partnership with Hwatsing). The research team consists of members from top research institutions such as Tsinghua University and has obtained several internationally acknowledged certificates, including SEMI S2, SEMI F47 and ISO9001.

Hwatsing

HWATSING 华海清科

Overview

CMP technology, one of the five crucial gordian techniques in IC fabrication processes, has been developed into 12-inch copper polishing equipment. It is Hwasting's mission to commercialize its research findings by putting them on an industrial production line.

Hwatsing's rapid development can be attributed to a strong support system, particularly in its finances, by the Tianjin municipal government, according to the company chairman.

Figure: Scientists at a Hwatsing laboratory; 2018.

Hwatsing

HWATSING 华海清科

Recent research

In recent years, Hwasting has increased its industrialization of products by constantly releasing new ones, including:

- the Universal-300 (the 12 inch copper polishing equipment);
- the Universal-150 (a small-size device);
- the Universal-150 Cluster (a polishing and cleaning machine); and
- the Universal-300 Plus (an updated version).

In 2015, six inventions and one utility model received patents.

In 2018, the Shanghai Huali Microelectronics Corporation, an IC foundry company, adopted Hwatsing's Cu&Si CMP equipment, which means the first home-made 12-inch copper process CMP equipment is being applied in the mass production line of integrated circuits.

To advance China's CMP technology in the semiconductor industry, Hwatsing Technology also recently developed the first commercial 12-inch dry-in/dry-out CMP equipment—Universal-300.

Hwatsing

HWATSING 华海清科

Recent research

Figure: The Hwatsing Universal-300 Plus

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Tsinghua University

Overview

Alongside its tie-up with Hwatsing for the express purpose of research leading to industrialization, Tsinghua University conducts concurrent CMP research.

In 2008, Tsinghua University Friction National Lab began to conduct research and technology development of CMP under super-low pressure. Two years later, Tsinghua University developed the first CMP sample machine. After multiple times of technological upgrading and iteration, the university succeeded in developing the 12-inch dry-in/dry-out CMP equipment in 2012, which is able to reduce surface roughness to less than 1nm on 12-inch wafer and reduce nonuniformity to below two percent (this, in partnership with Hwatsing, was later developed commercially). This equipment has made a milestone breakthrough in China's development of integrated circuit manufacturing equipment.

Figure: Tsinghua University laboratory

Tsinghua University

Additional information

CMP equipment technology, along with photo-etching, etching, ino implantation, and film growth, makes the core of the integrated circuit manufacturing techniques at Tsinghua's disposal.

So far, Hwatsing Technology and Tsinghua University have had more than 150 CMP technology-related patents and have primarily built a CMP equipment and technology system featuring technological advantage and intellectual property rights. Additionally, the university regularly publishes research papers on the topic, some of which are listed on the next page.

Selected publications

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Cabot

Overview

Headquartered in Aurora, Illinois, USA, Cabot Microelectronics Corporation (CMC) is the world's leading supplier of chemical mechanical planarization slurries (CMP) and second largest CMP pads supplier to the semiconductor industry.

Having started delving into research and commercialization in the 1980s, Cabot continues to be a hub for the research and advancement of Chemical Mechanical Planarization.

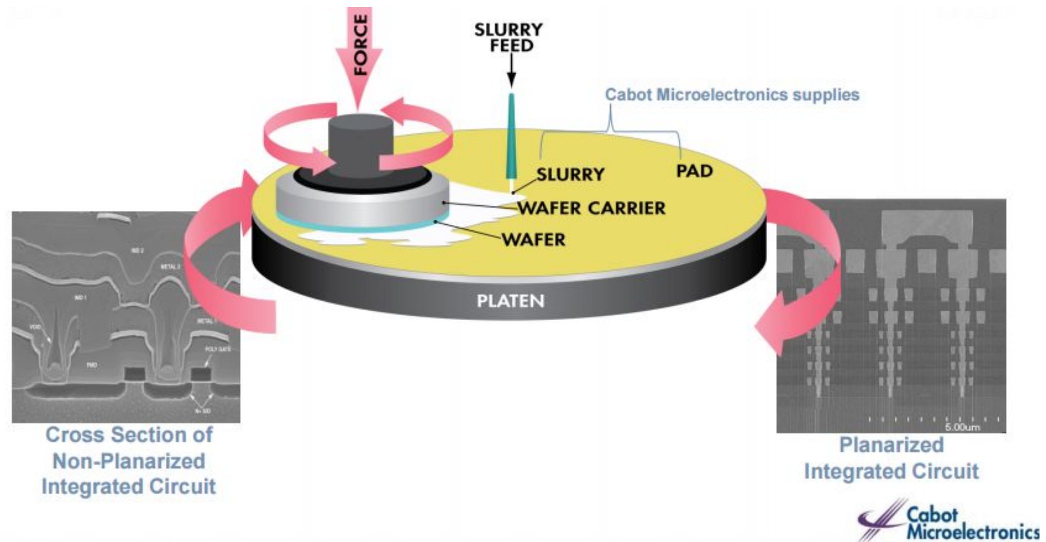

Figure: Cabot's CMP process

Cabot

Cabot Microelectronics

Patented technologies

CMP SLURRIES

As a pioneer in chemical mechanical planarization CMP slurries, Cabot commercialized its original research: the Semi-Sperse™ products in the 1980s for 250nm applications. With continuous improvement of some of these slurries, enhanced versions are still in use and key to customer solutions today, such as the flagship Semi-Sperse W2000 product for tungsten CMP.

Over the years, the company has successfully conducted research on and introduced a number of new CMP slurry platforms to meet our customers' evolving CMP needs, while reducing overall cost of ownership. For example, the company's iDIEL™ dielectric slurries utilizes engineered particles and unique chemistries to achieve improved planarity while significantly reducing defectivity.

Cabot

Cabot Microelectronics

Patented technologies

CMP POLISHING PADS

Developed in-house, Cabot's **Epic™** and **NexPlanar™** pads deliver a broad range of CMP polishing pad solutions, including performance-differentiated slurry and pad consumable sets. The **Epic™ CMP polishing pads** are the result of extensive research and development by CMC to deliver best-in-class performance at advanced technology nodes, quality improvements and optimal cost of ownership. Cabot Microelectronics designed and developed a patented thermoplastic technology for continuously manufacturing CMP pads. This unique, continuous manufacturing process has attracted many customers, as it has proven to successfully reduce pad-to-pad variation.

The **NexPlanar™ CMP polishing pads**, on the other hand, use proprietary formulation and fabrication methods – the very latest in modern chemistry and technology advances – to provide the customizable hardness, pore sizes, compressibility and groove patterns. Molded grooves eliminate the sharp edges and burrs, which results in improved defectivity. The NexPlanar pads also enable the low-stress CMP processing required for even the most advanced applications. Cabot's diverse line of advanced pad solutions compete on product performance, speed of iteration and lower cost of ownership, by reducing variability and improving yields.

Cabot

Cabot Microelectronics

Selected published technical papers

- Feeney, Paul. “CMP for metal-gate integration in advanced CMOS transfers.” 2010.
- Kamiti, M., Boldridge, D., Ndoping, L.M. and Remsen, E.E. “Simultaneous Absolute Determination of Particle Size and Effective Density of sub-Micron Colloids by Disc Centrifuge Photosedimentometry.”
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Clarkson University

Clarkson

Overview

Clarkson University is a research leader in the process of planarization (smoothing) of metal and dielectric films, primarily through its Center for Advanced Materials Processing (CAMP).

CAMP works with New York State companies as well as national and international companies who are interested in understanding and utilizing state-of-the-art advanced, tailor-designed materials and processes to improve their products, solve manufacturing challenges, increase yield, lower costs, and/or establish new or novel products.

The university regularly organizes events that focus on CMP topics such as:

- particle and colloidal aspects;
- polishing mechanisms;
- pad/conditioning behavior;
- flow characterization;
- copper/barrier film planarization;
- defects and post-polish cleaning;
- low-k films and integration challenges;
- 300 mm wafer issues and transition to 450 mm; and
- STI (shallow trench isolation).

Recent research

SURFACE SCRATCHES AND OTHER DEFECTS IN CMP PROCESSES

Hard abrasives such as silica and ceria can cause surface scratches and other defects in chemical mechanical planarization (CMP). In order to address this concern, softer polymer particles have been investigated as abrasives and/or complexing agents in CMP slurries. Researchers at Clarkson measured material removal rates (MRRs) of four different back end of line (BEOL) materials using slurries containing different concentrations of polymer particles using three types of polishing pads, and the interactions of the nanoparticles in the slurry with the pads were characterized.

Coefficient of friction measurements were performed in situ during polishing and the surface quality was studied before and after CMP using optical profilometry. Interestingly, an increase in the concentration of the polymer nanoparticles in the slurry resulted in an increase in the MRR for two of the four substrates evaluated, but a decrease in MRR for other two substrates. These changes were found to be related to the measured friction coefficients in the presence of the polymer particles. The goal of this work was to develop a mechanistic understanding of these effects.

Recent research (cont'd)

Figure: Scratching through the use of abrasive materials makes for a starkly different end product.

Clarkson

Recent research (cont.)

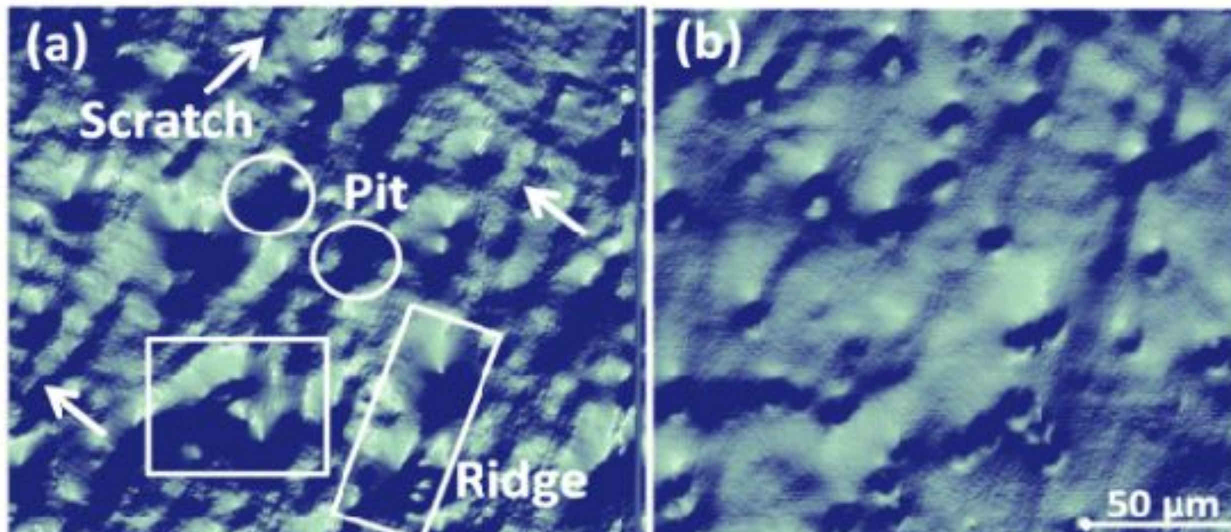

Figure: The surface profile of a scratched copper wafer.

Recent research (cont.)

The latex based slurries were found to significantly improve surface quality during the polishing of III-V substrate materials such as InP and InGaAs. The advent of new technology nodes with feature sizes below 10 nm has heightened the importance of avoiding or minimizing surface defect formation (defectivity) during CMP. The III-V semiconductors are attractive as high mobility channel materials for fast nMOS transistors.

Multiple CMP steps are usually required in the incorporation of these materials in device architectures. In the university's study on optimizing materials chemistry and process variables for CMP of 300-mm III-V blanket wafers, a systematic characterization and understanding of a range of surface defects became necessary, in addition to measuring the MRRs. Towards this end, a method based on high resolution optical profilometry and atomic force microscopy for characterizing these defects was developed.

Selected publications

- R. Bhonsle, L. Teugels, S. Ibrahim, P. Ong, M. Delande, S. Krishnan, M. Siebert, H. Struyf and L. Leunissen. "Inspection, Characterization and Classification of Defects for Improved CMP of III-V Materials," *ECS Journal of Solid State Science and Technology* 4 (11), P5073-P5077. 2015.
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Next Steps

SOME POSSIBILITIES THAT PRESCOUTER CAN OFFER FOR CONTINUATION OF OUR RELATIONSHIP

- COMPETITIVE INTELLIGENCE
- TECHNOLOGY ROADMAPPING
- TECHNOLOGY & PATENT LANDSCAPING
- MARKET RESEARCH & ANALYSIS
- TRENDS MAPPING
- REVIEW BEST PRACTICES
- PATENT COMMERCIALIZATION STRATEGY
- DATA ANALYSIS & RECOMMENDATIONS
- ACQUIRE NON-PUBLIC INFORMATION
- SUPPLIER OUTREACH & ANALYSIS
- CONSULT WITH INDUSTRY SUBJECT MATTER EXPERTS
- INTERVIEWING COMPANIES & EXPERTS

WE CAN ALSO DO THE FOLLOWING

- **CONFERENCE SUPPORT:** Attend conferences of interest on your behalf.
- **WRITING ARTICLES:** Write technical or more public facing articles on your behalf.
- **WORKING WITH A CONTRACT RESEARCH ORGANIZATION:** Engage with a CRO to build a prototype, test equipment or any other related research service.

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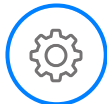

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